A-812PG

Hardware User's Manual

Warranty

All products manufactured by ICP DAS are warranted against defective materials for a period of one year from the date of delivery to the original purchaser.

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1. Introduction

1.1 General Description

The A-812PG is a high performance, multifunction analog, digital I/O board for the PC AT compatible computer. The A-812PG provides low gain (1, 2, 4, 8, 16). The A-812PG contains a 12-bit ADC with up to 16 single-ended analog inputs. The maximum sample rate of A/D converter is about 62.5 k sample/sec. There are two 12-bits DAC with voltage outputs, 16 channels of TTL-compatible digital input, 16 channels of TTL-compatible digital output and one 16-bit counter/timer channel for timing input and output.

1.2 Features

- The maximum sample rate of A/D converter is about 62.5 k sample/sec.
- Software selectable input ranges
- PC AT compatible ISA bus
- A/D trigger mode : software trigger , pacer trigger, external trigger
- 16 single-ended input signals
- Programmable low gain : 1,2,4,8,16
- 2 channel 12-bit D/A voltage output
- 16 digital input /16 digital output (TTL compatible)
- Interrupt handling
- 1 channel general purpose programmable 16 bits timer/counter

1.3 Specifications

Model Name	A-812PG
Analog Input	
Channels	16 single-ended
A/D Converter	12-bit, 8 µs conversion time
Sampling Rate	62.5 kS/s. max.
Over voltage Protection	Continuous +/-35 Vp-p
Input Impedance	10 MΩ/6 pF
Trigger Modes	Software, Pacer, external
Data Transfer	Polling, Interrupt, DMA
Accuracy	0.01 % of FSR ±1 LSB @ 25 °C, ± 10 V
Zero Drift	15 ppm/°C of FSR
Analog Output	
Channels	2 independent
Resolution	12-bit
Accuracy	0.01 % of FSR ± 1 LSB @ 25 °C, ± 10 V
Output Range	Unipolar: 0 ~ 5 V, 0 ~10 V Bipolar: +/-10 V
Output Driving	+/- 5 mA
Slew Rate	0.6 V/µs
Output Impedance	0.1 Ω max.
Operating Mode	Software
Digital Input	
Channels	16
Compatibility	5 V/TTL
Input Voltage	Logic 0: 0.8 V max. Logic 1: 2.0 V min.
Response Speed	1.0 MHz (Typical)
Digital Output	
Channels	16
Compatibility	5 V/TTL
Output Voltage	Logic 0: 0.4 V max. Logic 1: 2.4 V min.
Output Capability	Sink: 0.8 mA @ 0.8 V Source: -2.4 mA @ 2.0 V
Response Speed	1.0 MHz (Typical)
Timer/Counter	
Channels	3 independent
Resolution	16-bit
Compatibility	5 V/TTL
Input Frequency	10 MHz max.
Reference Clock	Internal: 2 MHz
General	
Bus Type	ISA
I/O Connector	20-pin box header x 5
Dimensions (L x W x D)	163 mm x 124 mm x 22 mm
Power Consumption	960 mA @ +5 V
Operating Temperature	0 ~ 60 °C
Storage Temperature	-20 ~ 70 °C
Humidity	5 ~ 85% RH, non-condensing

- Analog Input Range : (software programmable)

Model	**A-812PG**					
Gain	0.5	1	2	4	8	16
Bipolar (V)	+/-10	+/- 5	+/- 2.5	+/- 1.25	+/- 0.625	+/- 0.3125
Sampling Rate Max.	62.5 kS/s					

(Input Range : ±10 V or ±0.3125 V by Jumper JP4 selected)

1.3.1 Direct Memory Access Channel (DMA)

- Level : CH1 or CH3, jumper selectable
- Enable : via DMA bit of control register
- Termination : by interrupt on T/C
- Transfer rate : 100 k conversions/sec.

1.4 Applications

- Signal analysis
- FFT & frequency analysis
- Transient analysis
- Production test
- Process control
- Vibration analysis
- Energy management
- Industrial and lab. measurement and control

1.5 Product Check List

The package includes the following items:

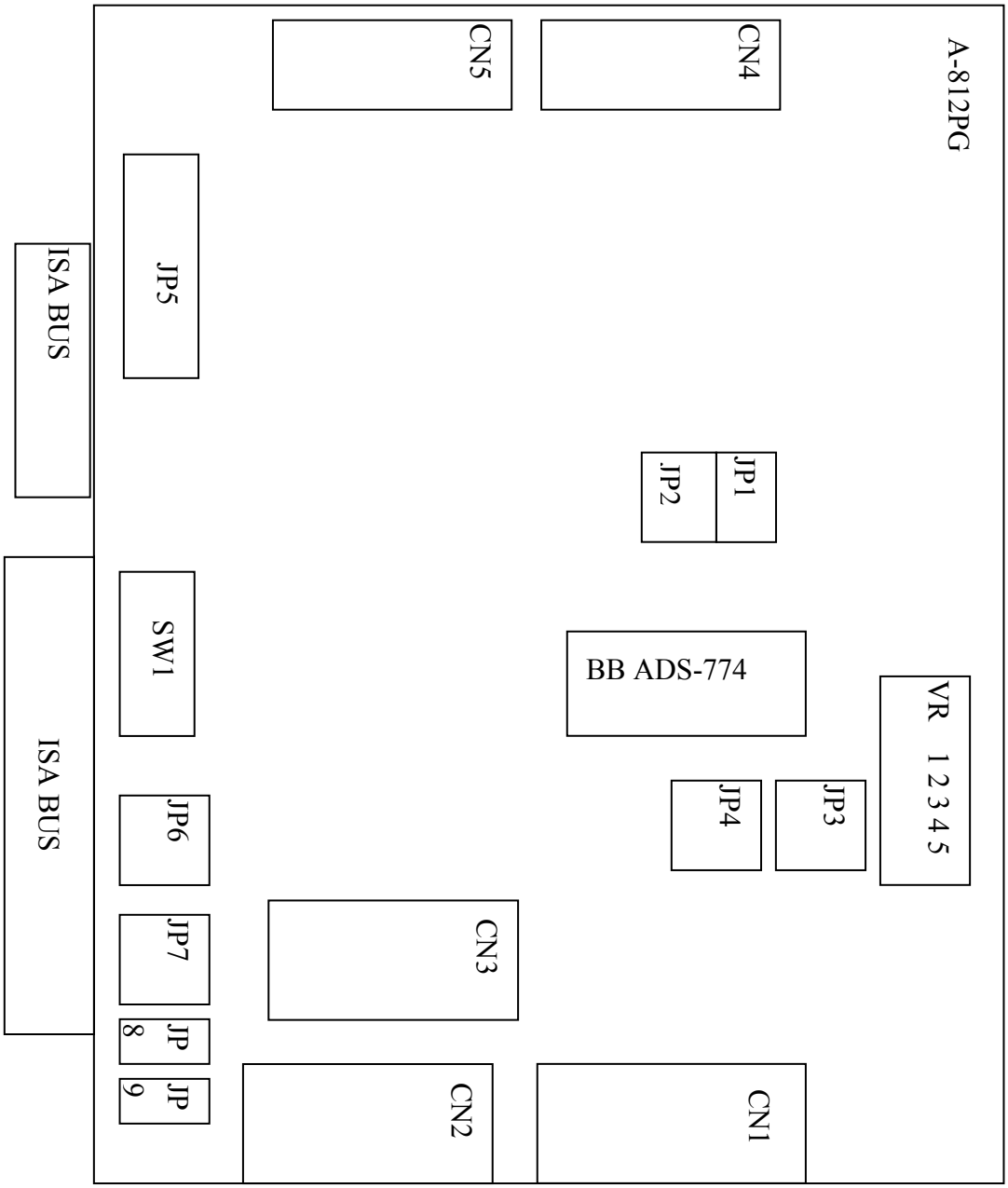
- One piece of A-812PG multifunction card
- One company floppy diskette or CD
- One Quick Start Guide

Attention !

If any of these items is missing or damaged, contact the dealer who provides you this product. Save the shipping materials and carton in case you want to ship or store the product in the future.

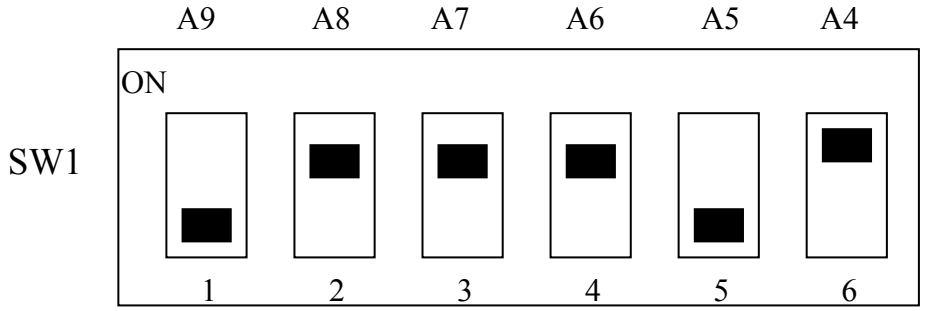
2. Hardware Configuration

2.1 Board Layout



2.2 I/O Base Address Setting

The A-812PG occupies 16 consecutive locations in I/O address space. The base address is set by DIP switch SW1. The default address is 0x220.



Default Base Address 220 Hex

For Example

How to select 2 2 0 (Hex)

OFF → 1
ON → 0

	2		2				0
	OFF	ON	ON	ON	OFF	ON	
→	1	0	0	0	1	0	
	A9	A8	A7	A6	A5	A4	

The detail SW1 base addresses setting. Please refer to **2.2.1 Base Address Table.**

2.2.1 Base Address Table

(*): Default base address

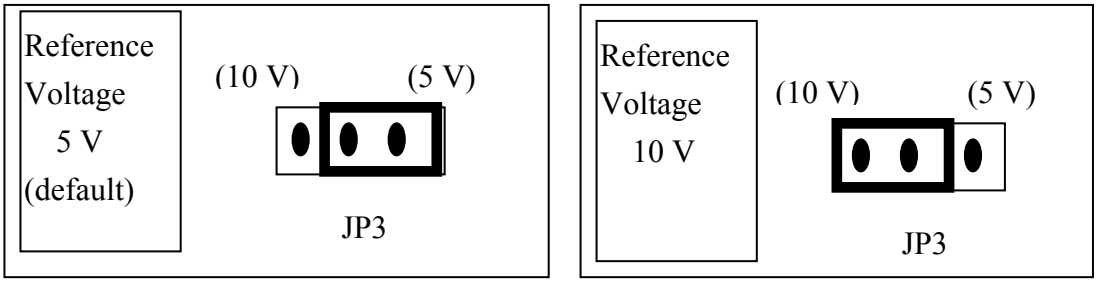
Base Adders	1 A9	2 A8	3 A7	4 A6	5 A5	6 A4
200-20F	OFF	ON	ON	ON	ON	ON
210-21F	OFF	ON	ON	ON	ON	OFF
220-22F (*)	**OFF**	**ON**	**ON**	**ON**	**OFF**	**ON**
230-23F	OFF	ON	ON	ON	OFF	OFF
240-24F	OFF	ON	ON	OFF	ON	ON
250-25F	OFF	ON	ON	OFF	ON	OFF
260-26F	OFF	ON	ON	OFF	OFF	ON
270-27F	OFF	ON	ON	OFF	OFF	OFF
280-28F	OFF	ON	OFF	ON	ON	ON
290-29F	OFF	ON	OFF	ON	ON	OFF
2A0-2AF	OFF	ON	OFF	ON	OFF	ON
2B0-2BF	OFF	ON	OFF	ON	OFF	OFF
2C0-2CF	OFF	ON	OFF	OFF	ON	ON
2D0-2DF	OFF	ON	OFF	OFF	ON	OFF
2E0-2EF	OFF	ON	OFF	OFF	OFF	ON
2F0-2FF	OFF	ON	OFF	OFF	OFF	OFF
300-30F	OFF	OFF	ON	ON	ON	ON
310-31F	OFF	OFF	ON	ON	ON	OFF
320-32F	OFF	OFF	ON	ON	OFF	ON
330-33F	OFF	OFF	ON	ON	OFF	OFF
340-34F	OFF	OFF	ON	OFF	ON	ON
350-35F	OFF	OFF	ON	OFF	ON	OFF
360-36F	OFF	OFF	ON	OFF	OFF	ON
370-37F	OFF	OFF	ON	OFF	OFF	OFF
380-38F	OFF	OFF	OFF	ON	ON	ON
390-39F	OFF	OFF	OFF	ON	ON	OFF
3A0-3AF	OFF	OFF	OFF	ON	OFF	ON
3B0-3BF	OFF	OFF	OFF	ON	OFF	OFF
3C0-3CF	OFF	OFF	OFF	OFF	ON	ON
3D0-3DF	OFF	OFF	OFF	OFF	ON	OFF
3E0-3EF	OFF	OFF	OFF	OFF	OFF	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF

The PC I/O port mapping is given below.

ADDRESS	Device	ADDRESS	Device
000-1FF	PC reserved	320-32F	XT Hard Disk
200-20F	Game/control	378-37F	Parallel Printer
210-21F	XT Expansion Unit	380-38F	SDLC
238-23F	Bus Mouse/Alt. Bus Mouse	3A0-3AF	SDLC
278-27F	Parallel Printer	3B0-3BF	MDA/Parallel Printer
2B0-2DF	EGA	3C0-3CF	EGA
2E0-2E7	AT GPIB	3D0-3DF	CGA
2E8-2EF	Serial Port	3E8-3EF	Serial Port
2F8-2FF	Serial Port	3F0-3F7	Floppy Disk
300-31F	Prototype Card	3F8-3FF	Serial Port

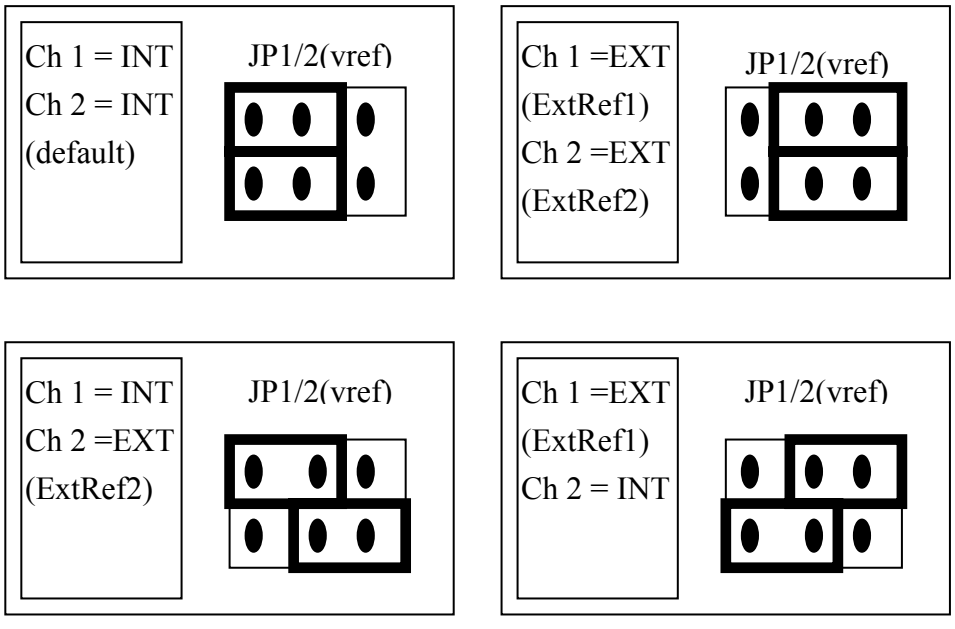
2.3 Jumper Setting

2.3.1 JP3 : D/A Internal Reference Voltage Selection



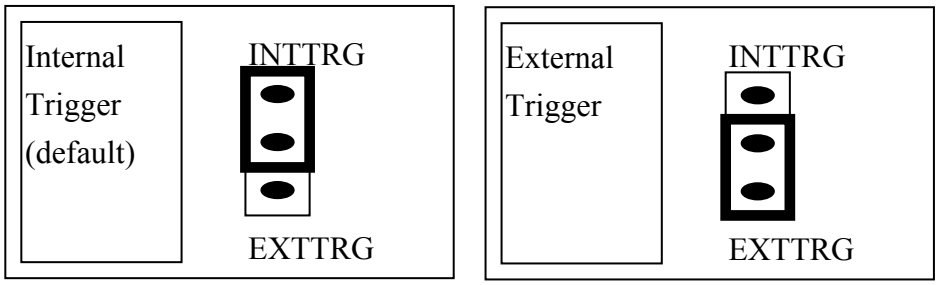
Select (5 V) : D/A voltage output = 0 ~ 5 V (both channel)
Select (10 V) : D/A voltage output = 0 ~ 10 V (both channel)
JP3 is validate only if JP1/JP2 select D/A internal reference voltage

2.3.2 JP1, JP2 : D/A Int/Ext Ref Voltage Selection



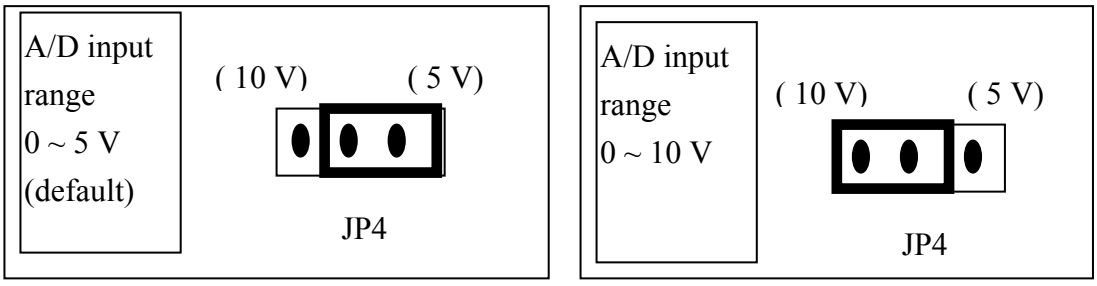
If JP1/2 select **internal reference**, then JP3 select **5 V/ 10 V** internal reference voltage. If JP1/2 select **external reference**, then **ExtRef1, CN2 pin 17**, is the external reference voltage for DA channel 1. and **ExtRef2, CN2 pin 19**, is the external reference voltage for DA Channel 2. If user provides AC +/- 10 V external reference voltage, the D/A output voltage may be AC -/+ 10 V

2.3.3 JP8 : A/D Trigger Source Selection



The A-812PG supports two trigger type, **internal trigger** and **external trigger.** The external trigger comes from **ExtTrg, CN3 pin 1**. There are two types of internal trigger, **software trigger** and **pacer trigge**r.

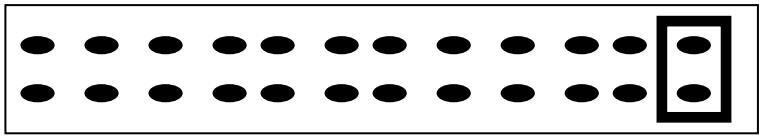
2.3.4 JP4 : A/D Input Range Selection



Select (5 V) : A/D voltage input = 0 ~ 5 V (total channel)
Select (10 V) : A/D voltage input = 0 ~ 10 V (total channel)

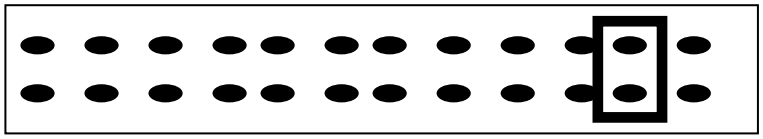
2.3.5 JP5 : Interrupt Level Selection

NO Interrupt



IRQ	3	4	5	6	7	9	10	11	12	14	15	NC

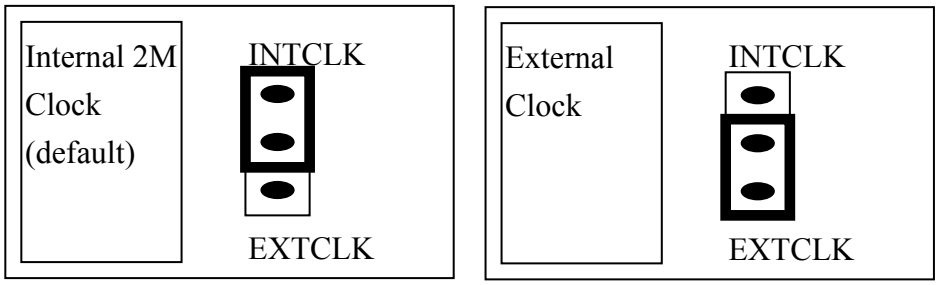
Interrupt 15
(default)



IRQ	3	4	5	6	7	9	10	11	12	14	15	NC

The interrupt channel **can not be shared.** The A-812PG software driver can support 8 different boards in one system but only **2 of these cards** can use interrupt transfer function.

2.3.6 JP9 : User Timer/Counter Clock Input Selection

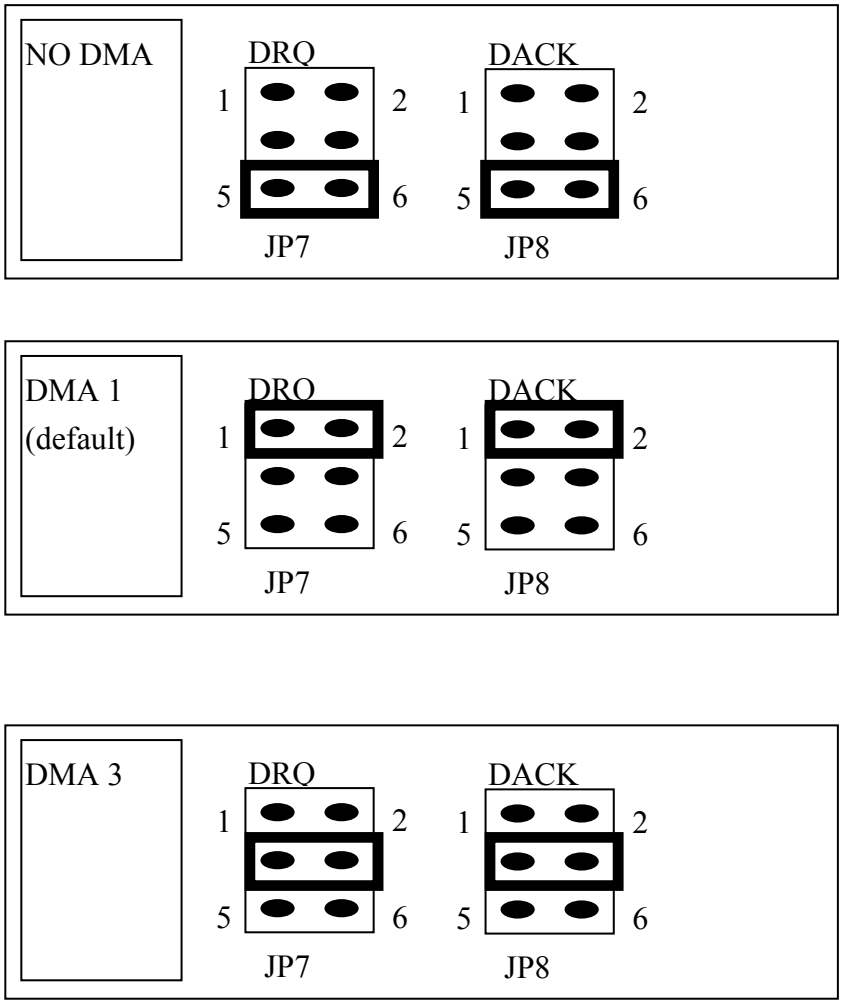


The A-812PG has 3 independent 16 bits timer/counter. The cascaded counter1 and counter2 are used as **pacer timer**. The counter0 can be used as a user programmable timer/counter. The user programmable timer/counter can select **2 M internal clock** or **external clock ExtCLK, CN3 pin 8**. The block diagram is given in section 2.6. The clock source must be very **stable.** It is recommended to use internal 2 M clock.

The A-812PG software driver uses the counter0 as a machine independent timer. If user program call **A-812PG_Delay()** subroutine, the counter0 will be programmed as a machine independent timer. The detail information is given in section 2.6.

2.3.7 JP6 : DMA DACK Selection,

JP7 : DMA DRQ Selection



The DMA channel cannot be shared. The A-812PG software driver can support 8 different boards in one PC based system, but only **two of these boards** can use DMA transfer function.

2.4 I/O Register Address

The A-812PG occupies 16 consecutive PC I/O addresses. The following table lists the registers and their locations.

Address	**Read**	**Write**
Base+0	8254 Counter 0	8254 Counter 0
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control
Base+4	A/D Low Byte	D/A Channel 0 Low Byte
Base+5	A/D High Byte	D/A Channel 0 High Byte
Base+6	DI Low Byte	D/A Channel 1 Low Byte
Base+7	DI High Byte	D/A Channel 1 High Byte
Base+8	Reserved	A/D Clear Interrupt Request
Base+9	Reserved	A/D Gain Control
Base+A	Reserved	A/D Multiplexer Control
Base+B	Reserved	A/D Mode Control
Base+C	Reserved	A/D Software Trigger Control
Base+D	Reserved	DO Low Byte
Base+E	Reserved	DO High Byte
Base+F	Reserved	Reserved

2.4.1 8254 Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about 8254, please refer to Intel‘s “Microsystem Components Handbook”.

Address	**Read**	**Write**
Base+0	8254 Counter 0	8254 Counter 0
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control

2.4.2 A/D Input Buffer Register

(READ) Base+4 : A/D Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+5 : A/D High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	READY	D11	D10	D9	D8

A/D 12 bits data : D11…..D0, D11=MSB, D0=LSB
READY =1 : A/D 12 bits data is not ready
=0 : A/D 12 bits data is ready

The low 8 bits A/D data are stored in address BASE+4 and the high 4 bits data are stored in address BASE+5. The READY bit is used as an indicator for A/D conversion. **When a A/D conversion is completed, the READY bit will be clear to zero.**

2.4.3 D/A Output Latch Register

(WRITE) Base+4 : Channel 1 D/A Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+5 : Channel 1 D/A High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D11	D10	D9	D8

(WRITE) Base+6 : Channel 2 D/A Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+7 : Channel 2 D/A High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D11	D10	D9	D8

D/A 12 bits output data : D11..D0, D11=MSB, D0=LSB, X=don‘t care

The D/A converter will convert the 12 bits digital data to analog output. The low 8 bits of **D/A channel 1** are stored in address BASE+4 and high 4 bits are stored in address BASE+5. The address BASE+6 and BASE+7 store the 12 bits data for **D/A channel 2**. The D/A output latch registers are designed as a **“double buffered”** structure, so the analog output latch registers will be updated until the high 4 bits digital data are written. If the user sends the high 4 bits data first, the DA 12 bits output latch registers will update at once. So the low 8 bits will be the previous data latched in register. **This action will cause an error on DA output voltage**. **So the user must send low 8 bits first and then send high 4 bits to update the 12 bits AD output** latch register.

NOTE : Send low 8 bits first, then send high 4 bits.

2.4.4 D/I Input Buffer Register

(READ) Base+6 : D/I Input Buffer Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+7 : D/I Input Buffer High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

D/I 16 bits input data : D15..D0, D15=MSB, D0=LSB

The A-812PG provides 16 TTL compatible digital inputs. The low 8 bits are stored in address BASE+6. The high 8 bits are stored in address BASE+7.

2.4.5 Clear Interrupt Request

(WRITE) Base+8 : Clear Interrupt Request Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don‘t care, XXXXXXXX=any 8 bits data is validate

If A-812PG is working in the interrupt transfer mode, an on-board hardware status bit will be set after each A/D conversion. This bit must be **clear by software** before the next hardware interrupt. Writing any value to address BASE+8 will clear this hardware bit and the hardware will generate another interrupt when next A/D conversion is completed.

2.4.6 A/D Gain Control Register

(WRITE) Base+9 : A/D Gain Control Register Format

y	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	GAIN2	GAIN1	GAIN0

The **A-812PG provides gain factor of 1/2/4/8/16.** The gain control register controls the gain of A/D input signal. JP4 A/D input selection will effect the gain factor.

NOTE : If gain control code changed, the hardware need to delay extra gain settling time. The gain settling time is different for different gain control code. **The software driver does not take care the gain settling time, so the user need to delay the gain settling time if gain changed.** If the application program need to run in different machines, the user need to implement a machine independent timer.

A-812PG GAIN CONTROL CODE TABLE

JP4 = 5 V

Settling Time	GAIN	Input Range	GAIN2	GAIN1	GAIN0
23 μs	1	+/- 5 V	0	0	0
23 μs	2	+/- 2.5 V	0	0	1
25 μs	4	+/- 1.25 V	0	1	0
28 μs	8	+/- 0.625 V	0	1	1
28 μs	16	+/- 0.3125 V	1	0	0

JP4 = 10 V

Settling Time	GAIN	Input Range	GAIN2	GAIN1	GAIN0
23 μs	1	+/- 10V	0	0	0
23 μs	2	+/- 5 V	0	0	1
25 μs	4	+/- 2.5 V	0	1	0
28 μs	8	+/- 1. 25 V	0	1	1
28 μs	16	+/- 0.625 V	1	0	0

2.4.7 A/D Multiplex Control Register

(WRITE) Base+A : A/D Multiplexer Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D3	D2	D1	D0

A/D input channel selection data = 4 bits : D3..D0, D3=MSB, D0=LSB, X=don‘t care

The A-812PG provides 16 single-ended analog input signals. D3..D0 select the active channel.

2.4.8 A/D Mode Control Register

(WRITE) Base+B : A/D Mode Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	D2	D1	D0

X=don‘t care

JP8 Select Internal Trigger							
Mode Select			Trigger Type		Transfer Type		
D2	D1	D0	Software Trig	Pacer Trig	Software	Interrupt	DMA
0	0	0	X	X	X	X	X
0	0	1	Select	X	Select	X	X
0	1	0	X	Select	X	X	Select
1	1	0	X	Select	Select	Select	X

X=disable

JP8 Select External Trigger						
Mode Select			Trigger Type	Transfer Type		
D2	D1	D0	External Trigger	Software	Interrupt	DMA
0	0	0	X	X	X	X
0	0	1	X	X	X	X
0	1	0	Select	X	X	Select
1	1	0	Select	Select	Select	X

The A/D conversion operation can be divided into 2 stages, **trigger stage and transfer stage**. The trigger stage will generate a trigger signal to A/D converter and the transfer stage will transfer the result to the CPU.

The trigger method may be **internal trigger** or **external trigger.** The internal trigger can be **software trigger** or **pacer trigger. The software trigger is very simple but can not control the sampling rate very precisely.** In software trigger mode, the program issues a software trigger command any time needed. Then the program will poll the A/D status bit until the ready bit is 0.

The pacer trigger can control the sampling rate very precisely. So the converted data can be used to reconstruct the waveform of analog input signal. In pacer trigger mode, the pacer timer will generate trigger signals to A/D converter periodic. These converted data can be transfer to the CPU by polling or interrupt or DMA transfer method.

The software driver provides three data transfer methods, **polling, interrupt and DMA.** The polling subroutine, A-812PG_AD_PollingVar() or A-812PG_AD_PollingArray(), set A/D mode control register to **0x01.** This control word means software trigger and polling transfer. The interrupt subroutine, A-812PG_AD_INT_START(…), set A/D mode control mode register to **ox06.** This control word means pacer trigger and interrupt transfer. The DMA subroutine, A-812PG_AD_DMA_START(…), set A/D mode control register to **0x02**. This control word means pacer trigger and DMA transfer.

2.4.9 A/D Software Trigger Control Register

(WRITE) Base+C : A/D Software Trigger Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don‘t care, XXXXXXXX=any 8 bits data is validate

The A/D converter can be triggered by software trigger or pacer trigger. Writing any value to address BASE+C will generate a trigger pulse to A/D converter and initiated an A/D conversion operation. The address BASE+5 offers a ready bit to indicate an A/D conversion complete.

The software driver uses this control word to detect the A-812PG hardware board. **The software initiates a software trigger and checks the ready bit**. If the ready bit cannot be cleared to zero in a fixed time, the software driver will return an error message. If the I/O BASE address setting error, the ready bit will not be cleared to zero. The software driver, **A-812PG_CheckAddress()**, use this method to detect the correctness of I/O BASE address setting.

2.4.10 D/O Output Latch Register

(WRITE) Base+D : D/O Output Latch Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+E : D/O Output Latch High Byte Data Format

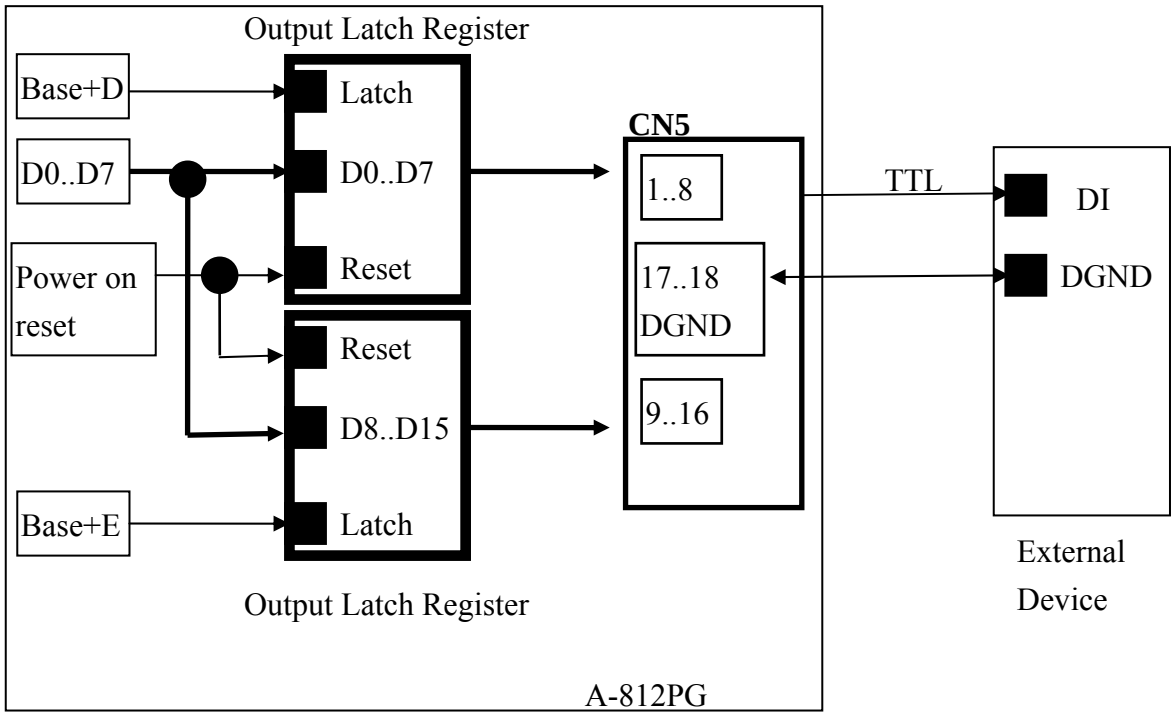
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

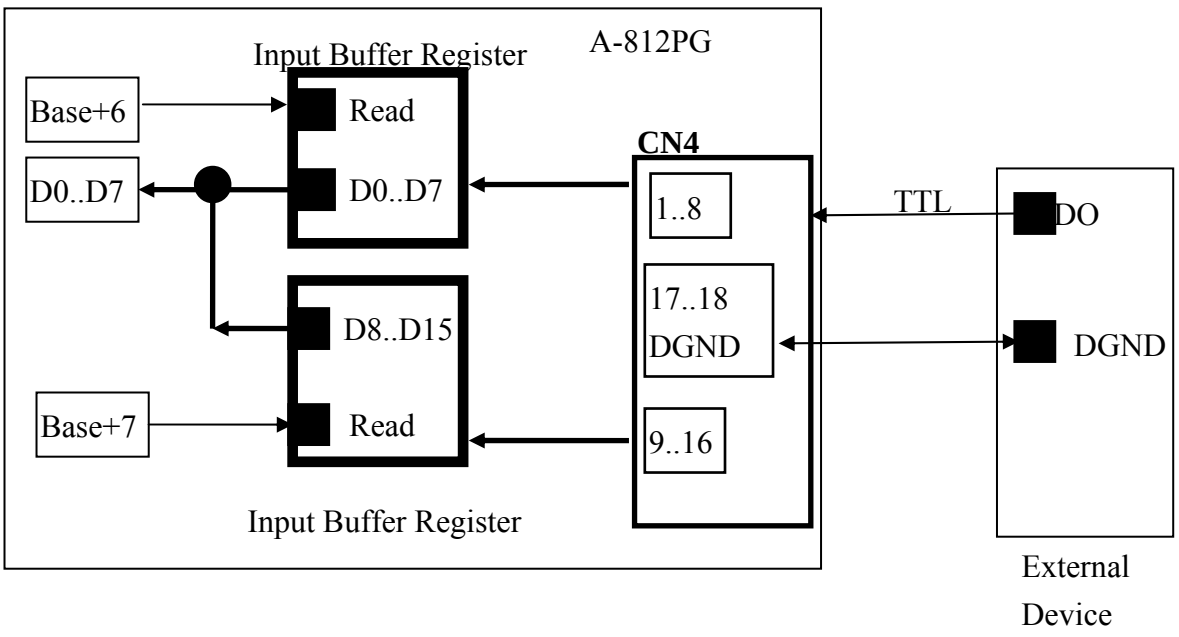
D/O 16 bits output data : D15..D0, D15=MSB, D0=LSB

The A-812PG provides 16 TTL compatible digital output. The low 8 bits are stored in address **BASE+D.** The high 8 bits are stored in address **BASE+E**

2.5 Digital I/O

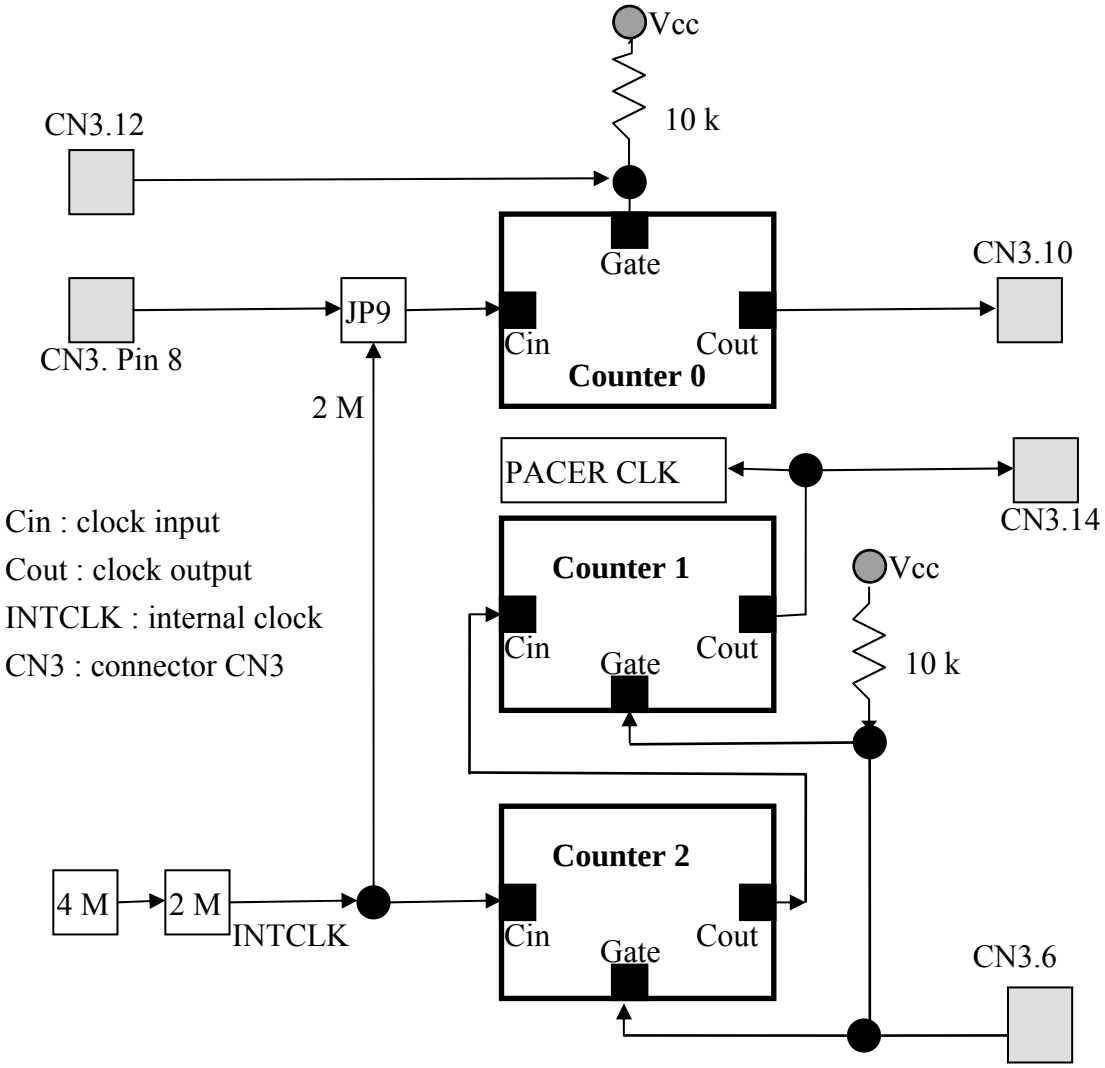
The A-812PG provides 16 digital input channels and 16 digital output channels. All levels are TTL compatible. The connections diagram and block diagram are given below:





2.6 8254 Timer/Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about 8254, please refer to Intel‘s “Microsystem Components Handbook”.The block diagram is as below.



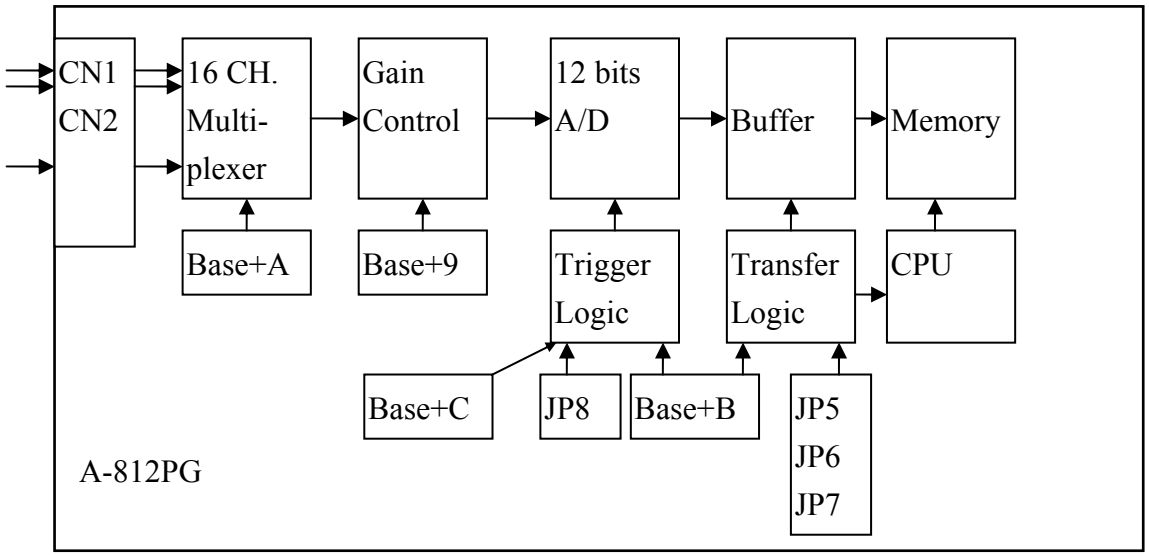
The counter0, counter1 and counter2 are all 16 bits counter. The counter1 and counter2 are cascaded as a 32 bits pacer timer. The counter0 is used as user timer/counter. The software driver use counter0 to implement a machine independent timer.

2.7 A/D Conversion

This section explains how to use A/D conversions. The A/D conversion can be triggered in any of 3 ways, **by software trigger, by pacer trigger or by external trigger** to the A/D converter. At the end of A/D conversion, it is possible to transfer data by one of 3 way, those are **polling, interrupt and DMA.** Before using the A/D conversion function, user should notice the following issue:

- A/D data register, BASE+4/BASE+5, store the A/D conversion data
- A/D gain control register, BASE+9, select gain
- A/D multiplex control register, BASE+A, select analog input
- A/D mode control register, BASE+B, select trigger type and transfer type A/D software trigger control register, BASE+C
- JP8 select internal/external trigger
- JP5 select IRQ level
- JP9 select internal/external clock for counter0
- JP6, JP7 select DMA channel
- **3 trigger logic : software, pacer, external trigger**
- **3 transfer logic : polling, interrupt, DMA**

The block diagram is given below:



2.7.1 A/D conversion flow

Before using the A/D converter, the user should setup the following hardware items :

1. Selects internal trigger or external trigger (JP8)
2. Selects IRQ level if needed (JP5)
3. Selects DMA channel if needed (JP6, JP7)
4. Selects internal clock or external clock for counter0 if needed (JP9)

Then the user must decide which A/D conversion mode will be used. The software driver supports three different modes: **polling, interrupt and DMA.** The user can control the A/D conversion by polling mode very easy. It is recommended to use the software driver if using interrupt or DMA mode.

The multiplexer can select one of the 16 single-ended channel and let external signal pass into the gain control module. T**he settling time of multiplexer depends on the source resistance.** Because the software **doesn't take care the settling time**, **the user should delay enough settling time if switching from one channel to next channel.**

The gain control module also need settling time if gain control code changed. Because the software **doesn't take care the settling time**, **the user should delay enough settling time if gain control code is changed.**

The software driver provides **a machine independent timer, A-812PG_Delay()**, for settling time delay. This subroutine assumes that JP6 select internal 2 M clock and use counter0 to implement a machine independent timer. If the user call A-812PG_delay(), the counter0 will be reserved and can't be used as a user programmable timer/counter.

The output of gain control module feed into the A/D converter. **The A/D converter needs a trigger signal to start an A/D conversion cycle**. The A-812PG supports three trigger mode, **software, pacer and external trigger**. The result of A/D conversion can be transfer into CPU by three mode : **polling, interrupt and DMA**.

2.7.2 A/D Conversion Trigger Modes

A-812PG supports three trigger modes.

1 : Software Trigger :

Writing any value to A/D software trigger control register, BASE+A, will initiate an A/D conversion cycle. This mode is very simple but very difficult to control sampling rate.

2 : Pacer Trigger Mode :

The pacer timer can give very precise sampling rate.

3 : External Trigger Mode :

When a rising edge of external trigger signal is applied, an A/D conversion will be performed. The external trigger source comes from pin 1 of CN3.

2.7.3 A/D Transfer Modes

A-812PG supports three transfer modes.

1 : Polling transfer :

This mode can be used with all trigger modes. The software scans A/D high byte data register, BASE+5, until READY_BIT=0.The low byte data is also ready in BASE+4.

2 : Interrupt transfer :

This mode can be used with pacer trigger or external trigger. The user can set the IRQ level by adjusting JP5. A hardware interrupt signal is sent to the PC when an A/D conversion is completed.

3 : DMA transfer :

This mode can be used with pacer trigger or external trigger. The user can set the DMA channel by adjusting JP6 and JP7. The hardware DMA request will send signals sequentially to the PC when an A/D conversion is completed. The single mode transfer of 8237 is suggested.

If using interrupt or DMA transfer, it is recommended to use A-812PG software driver.

2.7.4 Using software trigger and polling transfer

If the user needs to direct control the A/D converter without the A-812PG software driver. It is recommended to use software trigger and polling transfer. The program steps are listing as below:

1. Sends 0x01 to A/D mode control register (software trigger + polling transfer)
2. Sends channel number to multiplexer control register
3. Sends the gain control code value to gain control register
4. Delays the settling time
5. Sends any value to software trigger control register to generate a software rigger signal

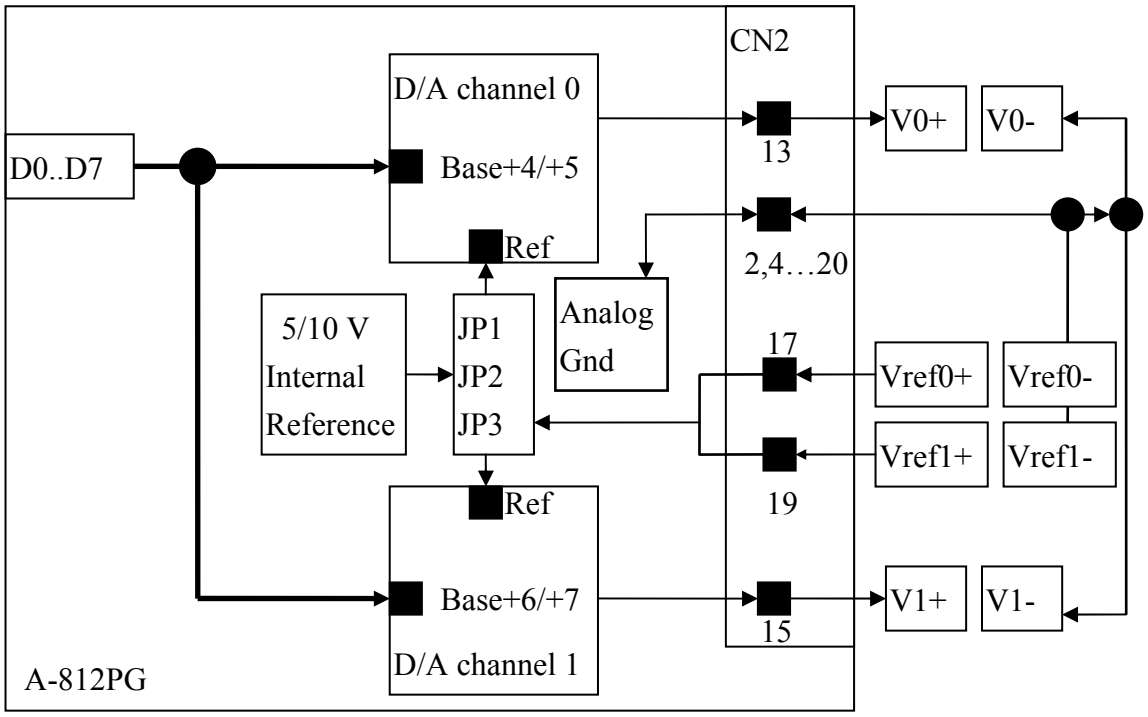
6. Scans the READY bit of the A/D high byte data until READY=0
7. Reads the 12 bits A/D data
8. Converts this 12 bits binary data to the floating point value

2.8 D/A Conversion

The A-812PG provides two 12 bits D/A converters. Before using the D/A conversion function, user should notice the following issue:

- D/A output register, BASE+4/BASE+5/BASE+6/BASE+7,
- JP3 select internal reference voltage 5 V/ 10 V
- JP1/JP2 select internal/external reference voltage
- If JP1/JP2 select internal and JP3 select 5 V, the D/A output range from 0 ~ 5 V
- If JP1/JP2 select internal and JP3 select 10 V, the D/A output range from 0 ~ 10 V
- If JP1/JP2 select external, the external reference voltage can be AC/DC +/- 10 V

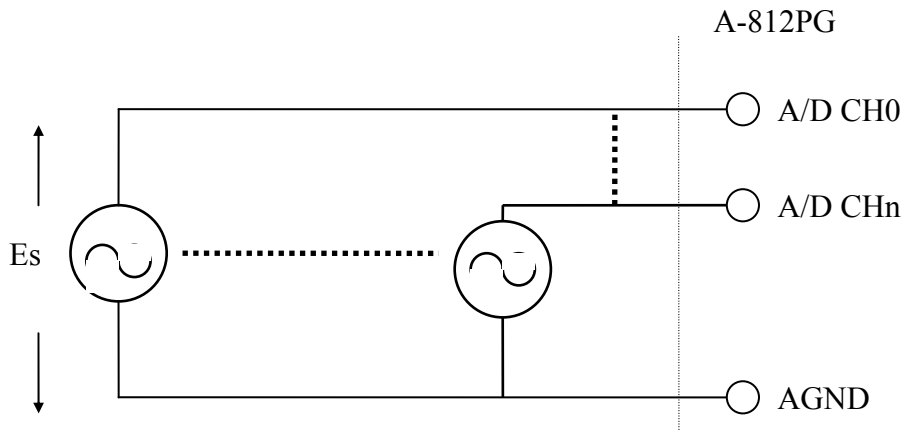
The block diagram is given as below:



NOTE : The DA output latch registers are designed as "double buffer" structure. **The user must send the low byte data first, then send the high byte data to store the DA 12 bits digital data**. If the user only sends the high byte data, then the low byte data will be still the previous value. Also if the user sends high byte first then send low byte, the low byte data of DA are still hold in the previous one.

2.9 Analog Input Signal Connection

FG1 : Connecting analog input configuration



2.10 Pin Assignment

CN1

AI 0	1	2	A.GND
AI 1	3	4	A.GND
AI 2	5	6	A.GND
AI 3	7	8	A.GND
AI 4	9	10	A.GND
AI 5	11	12	A.GND
AI 6	13	14	A.GND
AI 7	15	16	A.GND
AI 8	17	18	A.GND
AI 9	19	20	A.GND

CN2

AI10	1	2	A.GND
AI11	3	4	A.GND
AI12	5	6	A.GND
AI13	7	8	A.GND
AI14	9	10	A.GND
AI15	11	12	A.GND
AO 0	13	14	A.GND
AO 1	15	16	A.GND
AO 0 EXT REF	17	18	A.GND
AO 1 EXT REF	19	20	A.GND

Analog input connector

CN4

DI 0	1	2	DI 1
DI 2	3	4	DI 3
DI 4	5	6	DI 5
DI 6	7	8	DI 7
DI 8	9	10	DI 9
DI10	11	12	DI11
DI12	13	14	DI13
DI14	15	16	DI15
D.GND	17	18	D.GND
+5V	19	20	+12V

CN5

DO 0	1	2	DO 1
DO 2	3	4	DO 3
DO 4	5	6	DO 5
DO 6	7	8	DO 7
DO 8	9	10	DO 9
DO10	11	12	DO11
DO12	13	14	DO13
DO14	15	16	DO15
D.GND	17	18	D.GND
+5V	19	20	+12V

Digital input/output connector

CN3

External Trigger	1	2	N.C.
DRDY	3	4	N.C
Internal CLK 2MHz	5	6	Counter1 & 2 Gate
N.C.	7	8	External CLK
N.C.	9	10	Counter 0 Out
N.C.	11	12	Counter 0 Gate
N.C.	13	14	Counter 1 Out
N.C.	15	16	N.C.
D.GND.	17	18	Digital Ground
PC's+5V	19	20	N.C.

Timer/Counter connector

3. Daughter Board

The A-812PG can be connected with many different daughter boards. The functions of these daughter boards are described as follows.

3.1 DN-20 for Analog input / output

The DN-20 is a **general-purpose 20**-pin connector. This board can be connected to a 20-pin connector. It is suitable for easy signal connection and measurement.

3.2 DB-16P for Digital input

The DB-16P (or 782 series) is a **16-channel isolated digital input** board. The A-812PG provides 16-channel non-isolated TTL compatible digital inputs from CN4. If connecting to DB-16P, the A-812PG can provide 16 channels isolated digital input signals. Isolation can protect PC if abnormal input signal is occurred.

3.3 DB-16R for Digital output

The DB-16R (or 785 series) provides **16-channel SPDT relay output.** The A-812PG provides 16 channels TTL compatible digital output from CN5. If connecting to DB-16R, the A-812PG can provide 16 channels relay output to control power device.

4. Calibration

The A-812PG is calibrated to its best state of operation. For environment with large vibration, recalibration is recommended. Before calibrating the A-812PG, user should take care the following issue:

- One 6 digit multi-meter (DVM)
- One stable voltage source (4.9988 V)
- Diagnostic program: (A812DIAG.EXE) this program included in the delivered package will guide the user to proceed the calibration.

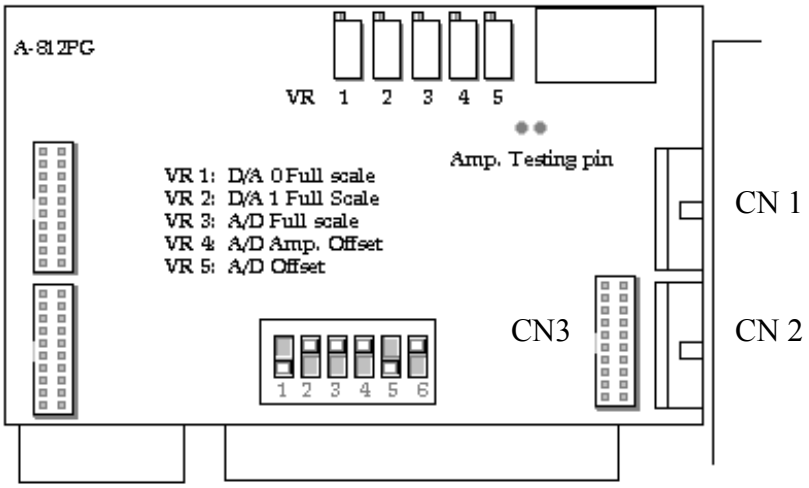


Fig. 3-1

4.1 Calibration VR Description

There are seven VRs on the A-812PG. Calibration need to adjust all seven VRs.

VR Num.	Description
VR1	D/A channel 0‘s gain adjustment
VR2	D/A channel 1‘s gain adjustment
VR3	A/D‘s gain adjustment
VR4	A/D's Amplifier offset adjustment
VR5	A/D‘s offset adjustment

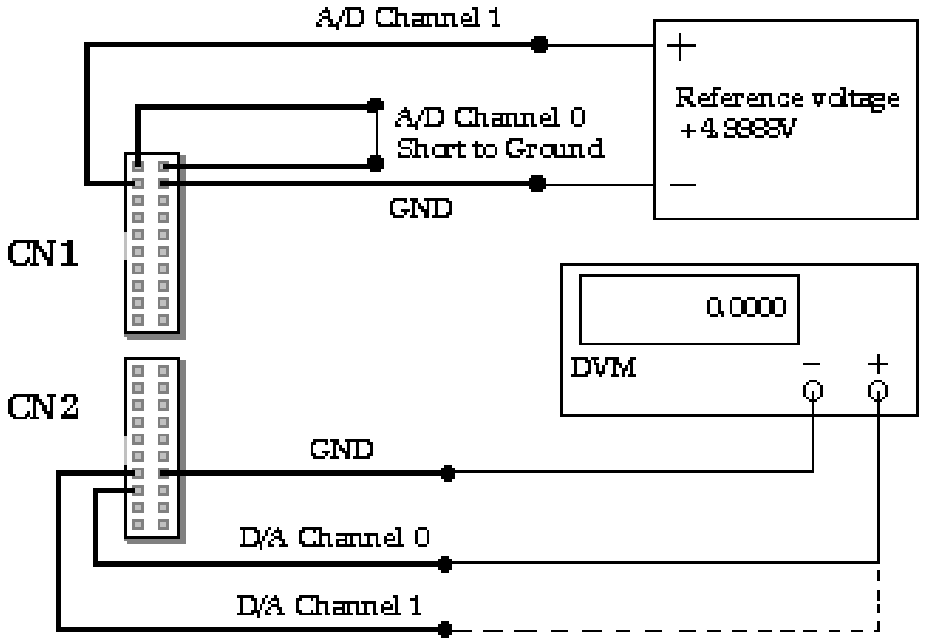


Fig. 3-2 Calibration wiring diagnostics

4.2 D/A Calibration Steps

1. Refer Fig. 3-2 Wiring diagnostics
2. Run A812DIAG.EXE
3. Press “Enter” key to start “CALIBRATION”
4. Connect CN2, pin 13 of CN2 (D/A Channel 0) and Pin 14 of CN2 (GND) to DVM (DC Voltage Meter)
5. Adjust VR1 until DVM=4.9988 V
6. Press “Enter" key
7. Connect D/A channel 1 Pin 15 of CN2 and Pin 14 of CN2 (GND) to DVM
8. Adjust VR2 until DVM=4.9988 V
9. Press “Enter" key

4.3 A/D Calibration Steps

1. Refer Fig3-2 wiring diagnostics
2. Run A812DIAG.exe
3. Press <Enter> key until A/D calibration start
4. Adjust VR5 until shower 4094/4095
5. Press <Enter>
6. Adjuster VR3 until shower 2047/2048
7. Press <Enter>
8. Repeater step 4 to step 7 until A/D channel 0 equal 2047/2048 and A/D channel 1 equal 4094/4095
9. Measure A/D Calibration is O.K. Press <Enter> Key until A/D Amp calibration is start
10. Adjust VR4 until A/D channel 0 equal 2047/8