

ISO-730

User Manual

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1. Introduction

The ISO-730 card provide 32 isolated digital I/O channels (16 x D/I and 16 x D/O) and 32 TTL-level digital I/O channels (16 x D/I and 16 x D/O). Each of the 16 isolated digital input channels accept voltage from 5 V ~ 30 V and has 1.2 k Ω resistance of. Every eight input channels use one external common ground. For example, channel 0~7 use EI.COM1 and channel 8~15 use EI.COM2. Each of the 16 isolated digital output channels equipped a darlington transistor. Every eight output channels use the external power. The channels 0~7 uses EO.COM1 and channels 8~15 use EO.COM2. The board interface to field logic signals, eliminating ground-loop problems and isolating the host computer from damaging voltages.

The ISO-730 has one 37-pin D-Sub connector and four on-board 20-pin flat-cable connectors. It is fully compatible to PCL-730.

1.1 Features and Applications

1.1.1 Features

- 16 isolated digital input channels
- 16 isolated open-collector output channels
- 16 non-isolated TTL inputs channels
- 16 non-isolated TTL outputs channels
- Interrupt level: 2,3,4,5,6,7 and jumper selectable.
- Current Sink for isolated Open Collector output (100 mA max.)
- Built-in DC/DC converter with 3000 VDC isolation
- 3750 Vrms photo-isolation protection
- One 37-pin D-sub connector and two 20-pin headers for isolated I/O
- Two 20-pin header for TTL digital I/O (Non-Isolation)

1.1.2 Applications

- Factory Automation
- Product Test
- Laboratory Automation

1.2 Product Check List

The shipping package includes the following items:

- One ISO-730 series card
- One software utility ISA CD.
- One Quick Start Guide.

It is recommended that you read the Quick Start Guide first. All the necessary and essential information is given in the Quick Start Guide, including:

- Where to get the software driver, demo programs and other resources.
- How to install the software.
- How to test the card.

Attention!

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Please save the shipping materials and carton in case you need to ship or store the product in the future.

1.3 Specifications

Model Name		ISO-730		
Digital Input				
Isolation Voltage		3750 Vrms		
Channala	Isolated	16		
Channels	Non-Isolated	16		
Compatibility	Isolated	Optical		
Compatibility	Non-Isolated	5 V/TTL		
	Isolated	Logic 0: DC 0 ~1 V		
Input Voltage		Logic 1: DC 9 ~ 24 V		
	Non-Isolated	L ogic 0: 0.8 V (max.) Logic 1: 2.0 V (min.)		
Input Impedance		1.2 KΩ, 0.5 W		
Deserves Oread	Isolated	10 kHz		
Response Speed	Non-Isolated	30 kHz		
Digital Output				
Isolation Voltage		3750 Vrms		
Channels	Isolated	16		
Channels	Non-Isolated	16		
Compatibility	Isolated	Sink, Open Collector		
Compatibility	Non-Isolated	5 V/TTL		
Output Voltage	Non-Isolated	Logic 0: 0.8 V (max.) Logic 1: 2.4 V (min.)		
	Isolate	Sink: 100 mA @ 30 Voc (max.)		
Output Capability	Non-Isolated	Sink: 8 mA @ 0.5 V (max.) Source: 0.4 mA @ 2.4 V (min.)		
Response Speed	Isolated	10 kHz		
General		·		
Bus Type		ISA		
1/O Connector		Female DB37 x 1		
		20-pin box header x 4		
Dimensions (L x W	/ x D)	175 mm x 124 mm x 22 mm		
Power Consumption	on	800 mA @ +5 V		
Operating Temper	ature	0 ~ 60 °C		
Storage Temperat	ure	-20 ~ 70 °C		
Humidity		5 ~ 85% RH, non-condensing		

2. Hardware Configuration

2.1 Board Layout



CN1	16-ch Isolated Open Collector Output					
CN2	16-ch Isolated Digital Input					
CN3	16-ch Digital Output					
CN4	16-ch Digital Input					
CN5	E.GND (External Ground)					
CN6	16-ch Isolated Input /16-ch Isolated Output					
JP1	Interrupt Level					
JP2	Interrupt Trigger					
JP3	Interrupt Source					
JP4,5	Version Control (A1,B2)					
SW1	Base Address					

2.2 I/O Board Address Setting

The ISO-730 occupies 4 consecutive I/O address space. The base address is set by DIP switch SW1. The default address is 0x300(hex).



(Default Base Address 300 Hex)

For Example

How to select 3 0 0 (Hex)

 $\begin{array}{l} \text{OFF} \rightarrow 1 \\ \text{ON} \rightarrow 0 \end{array}$

		3			0			
	OFF	OFF	ON	ON	ON	ON	ON	ON
>	1	1	0	0	0	0	0	0
	A9	A8	A7	A6	A5	A4	A3	A2

The detail SW1 base addresses setting. Please refer to **2.2.1 Base** Address Table.

Base Address	1	2	3	4	5	6	7	8
000	A9	A8	A7	A6	A5	A4	A3	A2
200		ON	ON	ON	ON	ON	ON	ON
204		ON	ON	ON	ON	ON	ON	OFF
208		ON	ON	ON	ON	ON		
200				ON	ON		OFF	OFF
210		ON	ON	ON	ON	OFF	ON	ON
214		ON	ON	ON	ON		ON	OFF
218		ON	ON	ON	ON	OFF		ON
210		ON	ON	ON	ON	OFF	OFF	OFF
220	OFF	ON	ON	ON	OFF	ON	ON	ON
224	OFF	ON	ON	ON	OFF	ON	ON	OFF
228	OFF	ON	ON	ON	OFF	ON	OFF	ON
22C	OFF	ON	ON	ON	OFF	ON	OFF	OFF
230	OFF	ON	ON	ON	OFF	OFF	ON	ON
234	OFF	ON	ON	ON	OFF	OFF	ON	OFF
238	OFF	ON	ON	ON	OFF	OFF	OFF	ON
23C	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
240	OFF	ON	ON	OFF	ON	ON	ON	ON
244	OFF	ON	ON	OFF	ON	ON	ON	OFF
248	OFF	ON	ON	OFF	ON	ON	OFF	ON
24C	OFF	ON	ON	OFF	ON	ON	OFF	OFF
250	OFF	ON	ON	OFF	ON	OFF	ON	ON
254	OFF	ON	ON	OFF	ON	OFF	ON	OFF
258	OFF	ON	ON	OFF	ON	OFF	OFF	ON
25C	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
260	OFF	ON	ON	OFF	OFF	ON	ON	ON
264	OFF	ON	ON	OFF	OFF	ON	ON	OFF
268	OFF	ON	ON	OFF	OFF	ON	OFF	ON
26C	OFF	ON	ON	OFF	OFF	ON	OFF	OFF
270	OFF	ON	ON	OFF	OFF	OFF	ON	ON
274	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
278	OFF	ON	ON	OFF	OFF	OFF	OFF	ON
27C	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
280	OFF	ON	OFF	ON	ON	ON	ON	ON
284	OFF	ON	OFF	ON	ON	ON	ON	OFF
288	OFF	ON	OFF	ON	ON	ON	OFF	ON
28C	OFF	ON	OFF	ON	ON	ON	OFF	OFF
290	OFF	ON	OFF	ON	ON	OFF	ON	ON
294	OFF	ON	OFF	ON	ON	OFF	ON	OFF
298	OFF	ON	OFF	ON	ON	OFF	OFF	ON
29C	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
2A0	OFF	ON	OFF	ON	OFF	ON	ON	ON
2A4	OFF	ON	OFF	ON	OFF	ON	ON	OFF
2A8	OFF	ON	OFF	ON	OFF	ON	OFF	ON
2AC	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
2B0	OFF	ON	OFF	ON	OFF	OFF	ON	ON
2B4	OFF	ON	OFF	ON	OFF	OFF	ON	OFF

2.2.1 Base Address Table:

0.5.0		.		.				.
2B8	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
2BC	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
2C0	OFF	ON	OFF	OFF	ON	ON	ON	ON
2C4	OFF	ON	OFF	OFF	ON	ON	ON	OFF
2C8	OFF	ON	OFF	OFF	ON	ON	OFF	ON
2CC	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
2D0	OFF	ON	OFF	OFF	ON	OFF	ON	ON
2D4	OFF	ON	OFF	OFF	ON	OFF	ON	OFF
2D8	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
2DC	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
2E0	OFF	ON	OFF	OFF	OFF	ON	ON	ON
2E4	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
2E8	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
2EC	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
2F0	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
2F4	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
2F8	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON
2FC	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
300(*)	OFF	OFE		ON	ON	ON	ON	
304	OFF	OFF						OFF
308	OFF	OFF					OFF	
300	OFF	OFF					OFF	OFF
310		OFF						
31/								
318								
310								
320								
320								
324								
320								
320								
334								
338								
330								
340								
340								
344								
340								
350								
354								
358								
350								
360								
364								
369								
360								
270								
370 274								
3/4 270								
370								
370								
380								
304 200								
300 200								
380				ON	UN	ON		

390	OFF	OFF	OFF	ON	ON	OFF	ON	ON
394	OFF	OFF	OFF	ON	ON	OFF	ON	OFF
398	OFF	OFF	OFF	ON	ON	OFF	OFF	ON
39C	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
3A0	OFF	OFF	OFF	ON	OFF	ON	ON	ON
3A4	OFF	OFF	OFF	ON	OFF	ON	ON	OFF
3A8	OFF	OFF	OFF	ON	OFF	ON	OFF	ON
3AC	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
3B0	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
3B4	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
3B8	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
3BC	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
3C0	OFF	OFF	OFF	OFF	ON	ON	ON	ON
3C4	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
3C8	OFF	OFF	OFF	OFF	ON	ON	OFF	ON
3CC	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
3D0	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
3D4	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
3D8	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
3DC	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
3E0	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
3E4	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF
3E8	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON
3EC	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
3F0	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
3F4	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
3F8	OFF	ON						
3FC	OFF							

(*): Default addresses setting

2.2.2 The I/O port mapping

I/O address	Device
0x000 ~ 0x1FF	PC reserved
0x200 ~ 0x20F	Game controller
0x278 ~ 0x27F	LPT2
0x2F8 ~ 0x2FF	COM2
0x300 ~ 0x31F	Prototype Card
0x320 ~ 0x32F	XT fixed disk
0x378 ~ 0x37F	LPT2
0x380 ~ 0x38F	SDLC
0x3A0 ~ 0x3AF	SDLE
0x3B0 ~ 0x3BF	Monochrome card
0x3C0 ~ 0x3CF	EGA card
0x3D0 ~ 0x3DF	CGA card
0x3F0 ~ 0xFF	Diskette controller, COM1

2.3 Jumper Setting

2.3.1 JP1 Interrupt Level

Using JP1 to select interrupt level from IRQ2 to IRQ7, as shown below.



2.3.2 JP2 Interrupt Trigger

Using JP2 to select the trigger edge on which the ISO-730 will trigger an interrupt.



2.3.3 JP3 Interrupt Source

Using JP3 to select the source of the interrupt.



Select	D/I channel	Connector
IDI0	Isolated D/I channel 0	CN2 Pin 1 or CN6 Pin 1
IDI1	Isolated D/I channel 1	CN2 Pin 2 or CN6 Pin 20
DIO	TTL D/I channel 0	CN4 Pin 1
DI1	TTL D/I channel 1	CN4 PIN 2

2.3.4 JP4/JP5 Version selection

The JP4 and JP5 control the pin assignment of CN1, CN2 and CN6. Make sure your setting first.



2.4 Pin Assignment

Before you use ISO-730, please make sure JP5/ JP4 position is in A1 or B2.

2.4.1 Pin-Assignment of B2 Version



CN6: 37-pin D-sub connector

CN1 / CN2 Pin-Assignment

	CN2			CN1
IDI 0 1 IDI 2 3 IDI 4 5 IDI 6 7 IDI 8 9 IDI10 11 IDI12 13 IDI14 15 EI.COM 19		2 4 6 8 10 12 14 16 18 20	IDI 1 IDI 3 IDI 5 IDI 7 IDI 9 IDI11 IDI13 IDI15 EI.COM EI.COM	IDO 0 1 OO 2 IDO 1 IDO 2 3 OO 4 IDO 3 IDO 4 5 OO 6 IDO 5 IDO 6 7 OO 8 IDO 7 IDO 8 9 OO 10 IDO 9 IDO10 11 OO 12 IDO11 IDO12 13 OO 14 IDO13 IDO14 15 OO 18 EO.GND EO.COM1 19 OO 20 EO.COM2

Isolated Digital input/output (B2)

2.4.2 Pin-Assignment of A1 Version

CN6 Pin-Assignment of A1 version



CN1 / CN6 Pin-Assignment of A1 Version

		CN2				(CN1		
IDI 0 IDI 2 IDI 4 IDI 6 IDI 8 IDI10 IDI12 IDI14 EI.COM	1 5 7 9 11 13 15 17 19	000000000000000000000000000000000000000	2 4 6 8 10 12 14 16 18 20	IDI 1 IDI 3 IDI 5 IDI 7 IDI 9 IDI11 IDI13 IDI15 EI.COM EI.COM	IDO 0 IDO 2 IDO 4 IDO 6 IDO 8 IDO10 IDO12 IDO14 EO.GND	1 3 7 9 11 13 15 17	000000000000000000000000000000000000000	2 4 8 10 12 14 16 18 20	IDO 1 IDO 3 IDO 5 IDO 7 IDO 9 IDO11 IDO13 IDO15 EO.GND EO.COM

Isolated Digital input/output (A1)

2.4.3 TTL I/O Pin-Assignment of CN4 / CN3

The CN4 and CN3 are TTL Level Digital Input/Output ports. It can accept DB-16P and DB-16R series daughter board or other TTL Level signals.



Digital input/output connector

2.5 Digital Input/Output

2.5.1 Isolated Input (CN2/CN6)

The ISO-730 provides 16-channel isolated digital inputs. Each of the 16 isolated digital inputs accepts voltages from $9 \sim 24 \text{ V}_{DC}$. Every eight input channels share one external ground.

Channels 0~7 use EI.COM1, Channels 8~15 use EI.COM2 (B2 Version)



2.5.2 Isolated Open-collector Output

Every eight open-collector output channels share EO.COM. (Channel 0~7 use EO.COM1, channel 8~15 use EO.COM2)

The maximum load of each channel is 100 mA/30 V(max.). If the current of each channel exceeds 150 mA, please use the connector CN5 to return the current to the external power.



(Recommend : It Is necessary to connect a diode1 (..3..) . In the External Device end as means of preventing damage form the counter emf . If your Device Is Inductive Load , Ex. Relay …)

2.5.3 TTL Digital I/O

The ISO-730 provides 16 TTL level digital input channels and 16 TTL level digital output channels.



3. I/O Register Address

The ISO-730 card occupies 4 consecutive I/O addresses. The registers and their locations is shown in the following table.

ISO-730 Address Register:

Address	Read	Write
Base+0	IDI Channel 0~7	IDO Channel 0~7
Base+1	IDI Channel 8~15	IDO Channel 8~15
Base+2	DI Channel 0~7	DO Channel 0~7
Base+3	DI Channel 8~15	DO Channel 8~15

IDI: Isolated Digital inputIDO: Isolated Open Collector OutputDI: TTL Digital InputDO: TTL Digital Output

The I/O channel of ISO-730 corresponds to a bit in the registers of the card. The channels and their register is shown in the following table.

Read/Write Base+0			(Isolated Digital I/O)						
Bit	7	6	5	4	3	2	1	0	
Channel	7	6	5	4	3	2	1	0	
Read/Write Base+1 (Isolated Digital I/O)									
Bit	7	6	5	4	3	2	1	0	
Channel	15	14	13	12	11	10	9	8	
Read/Write Base+2 (TTL Digital I/O)									
Bit	7	6	5	4	3	2	1	0	
Channel	7	6	5	4	3	2	1	0	
Read/Write Base+3 (TTL Digital I/O)									
Bit	7	6	5	4	3	2	1	0	
Channel	15	14	13	12	11	10	9	8	

For C Language:

```
Main()
{
int lo_add = 0x300; /* 730 I/O Address = 0x200 Default setting */
int ln_p0,ln_p1, ln_p2,ln_p3;
outportb( lo_add+0 , 0xaa ); /* output data '1010 1010' to con2 ID/O Channel 0~7 */
outportb( lo_add+1 , 0x55); /* output data '0101 0101' to con2 ID/O Channel 8~15 */
outportb( lo_add+2 , 0xaa ); /* output data '1010 1010' to con1 D/O Channel 0~7*/
outportb( lo_add+3 , 0x55); /* output data '0101 0101' to con1 D/O Channel 0~7*/
outportb( lo_add+3 , 0x55); /* output data '0101 0101' to con1 D/O Channel 8~15 */
In_p0=Inportb(lo_add+0); /* Read CON 2 ID/I Channel 0~7 Data */
In_p1=Inportb(lo_add+1); /* Read CON 2 ID/I Channel 8~15 Data */
In_p3=Inportb(lo_add+3); /* Read CON 1 D/I Channel 8~15 Data */
}
```

For Quick Basic Language

Bas=&h300							
OUT Bas+0, &HAA	' output data '1010 1010' to CON 2 ID/O Channel 0~7						
OUT Bas+1, &H55	' output data '0101 0101' to CON 2 ID/O Channel 8~15						
OUT Bas+2, &HAA	' output data '1010 1010' to CON 1 D/O Channel 0~7						
OUT Bas+3, &H55	' output data '0101 0101' to CON 1 D/O Channel 8~15						
P0=inp(Bas+0)	' Read CON 2 ID/I Channel 0~7 data						
P1=inp(Bas+1)	' Read CON 2 ID/I Channel 8~15 data						
P2=inp(Bas+2)	' Read CON 1 D/I Channel 0~7 data						
P3=inp(Bas+3)	' Read CON 1 D/I Channel 8~15 data						